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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,415	05/29/2001	Akiyuki Yoshisato	9281-3999	7090

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EXAMINER

DINH, TUAN T

ART UNIT PAPER NUMBER

2827

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/870,415

Applicant(s)

YOSHISATO ET AL.

Examiner

Tuan T Dinh

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 1-6 are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Claim Objections*

1. Claims 1, 3 are objected to because of the following informalities: Claims 1 and 3, line 4, change " a first transistor wire bonded" to --a first transistor including wire bonded--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Furutani et al. (U. S. Patent 5,561,592).

As to claim 1, Furutani discloses an electronic circuit unit as shown in figures 1-15 comprising:

thin film circuit elements including capacitors C, resistors R, and inductance L elements formed on an alumina substrate (column 1, line 38), and

a semiconductor bare chip (10-13) having a first transistor (11) including wire bonded to the alumina substrate (see figures 6-9),

wherein only an emitter resistor (R27, column 7, line 48), out of a base bias voltage dividing resistor (R24-R26) and the emitter resistor of the first transistor, is trimmed to set a current value of the first transistor.

As to claim 2, Furutani discloses the unit as shown in figures 6-9 wherein the semiconductor bare chip has a second transistor (12) connected to the first transistor (11) in series, and only the emitter resistor (27) of the first transistor, out of base bias voltage dividing resistors (24-26) and emitter resistors of the first and second transistors (11-12), is trimmed to set the current value of the first and second transistors.

As to claim 3, Furutani discloses the unit as shown in figures 1-10 comprising: circuit elements including thin film capacitors C, resistors R, and inductance L elements formed on an alumina substrate (column 1, line 38), and a semiconductor bare chip (10; 11; 12; 13) having a first transistor including wire bonded to the alumina substrate (see figures 6-8),

wherein thin film base bias voltage dividing resistor (R24-R26) to apply a voltage to a base of the first transistor are formed proximate to each other on the alumina substrate.

As to claim 4, Furutani discloses the unit wherein the semiconductor bare chip has a second transistor (12-figure 9) connected to the first transistor in series, and thin film base bias voltage dividing resistors of the first and second transistors are formed proximate to each other on the alumina substrate.

As to claims 5-6, Furutani discloses the unit as shown in figure 9 wherein at least a part of the base bias voltage dividing resistors (R24-R26) are located on a plurality of lines in parallel.

**Conclusion**

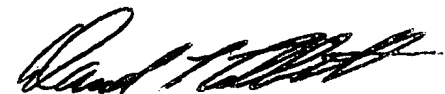
4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Crabill, Nakatsuka et al., Matsuno, and Kohjino et al. disclose related srt.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD  
April 7, 2003



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